A 50nm Depleted-Substrate CMOS Transistor (DST)

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Components Research

Logic Technology Development

Intel Corporation

Outline of Presentation

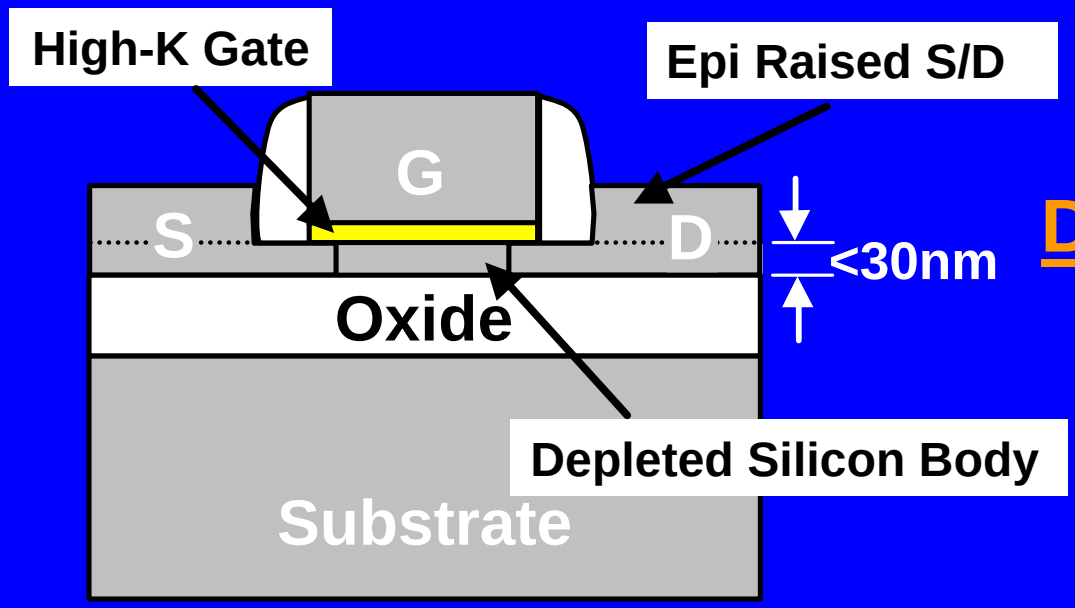
- Introduction
- DST Architecture
- Objective of This Work
- Process Flow
- Short Channel Effects and Transistor Performance
- Comparison to Bulk Si and P-D SOI
- Summary

Problem Statement

Transistor scaling issues

- Degradation in subthreshold slope (Bulk Si and P-D SOI)
- Increase in I_{OFF} (Bulk Si and P-D SOI)
- Degradation in DIBL (Bulk Si and P-D SOI)
- Increase in gate leakage (Bulk Si and P-D SOI)
- Increase in junction edge leakage (Bulk Si)

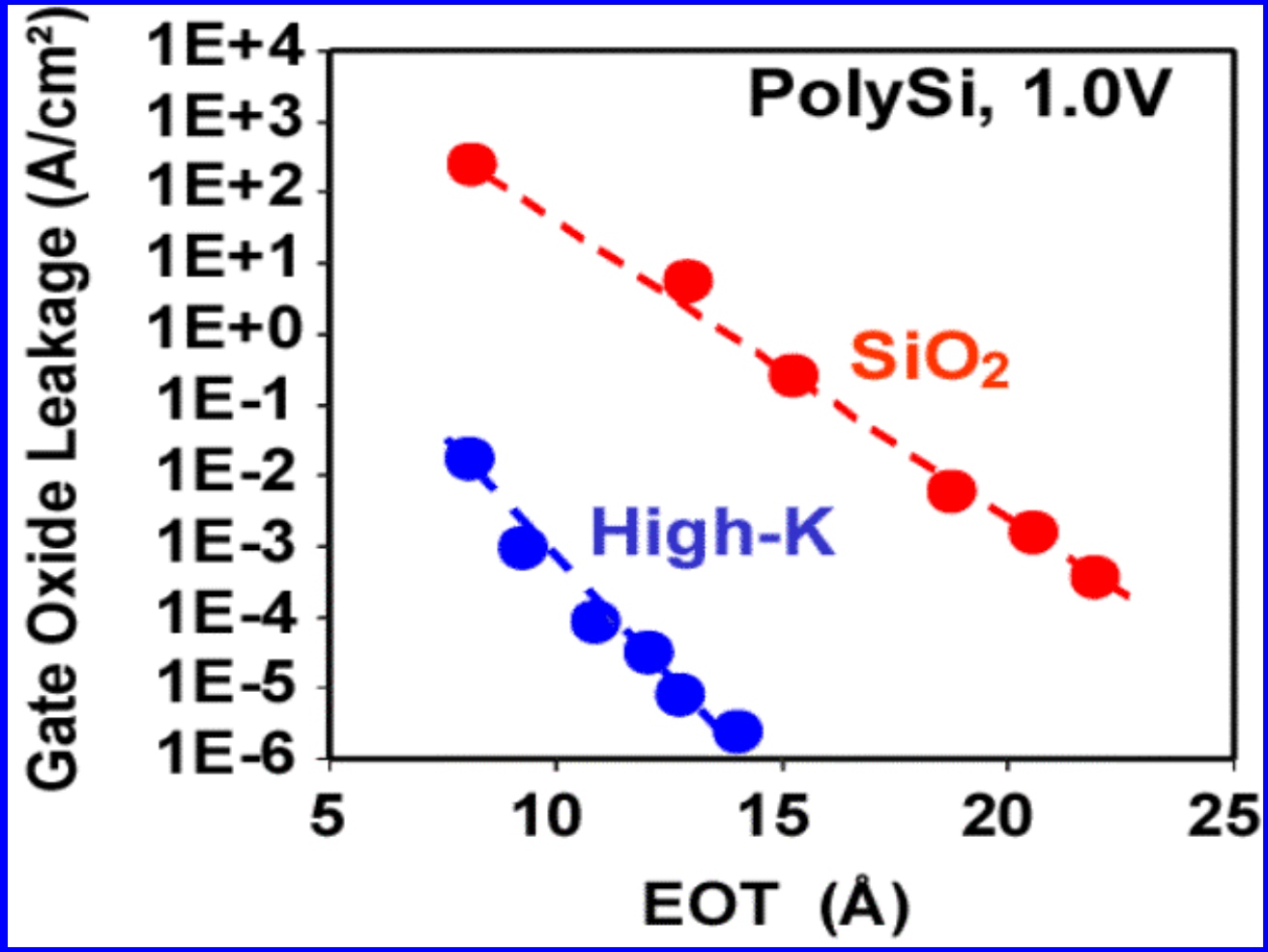
New Transistor Architecture



Depleted Substrate Transistor (DST)

- **High-K gate dielectric**
  - Reduce gate leakage
- **Depleted Silicon body**
  - Improve subthreshold slope and DIBL
- **Epi raised source-drain**
  - Reduce parasitic resistances and improve I_{ON}

High-K to Reduce Gate Leakage



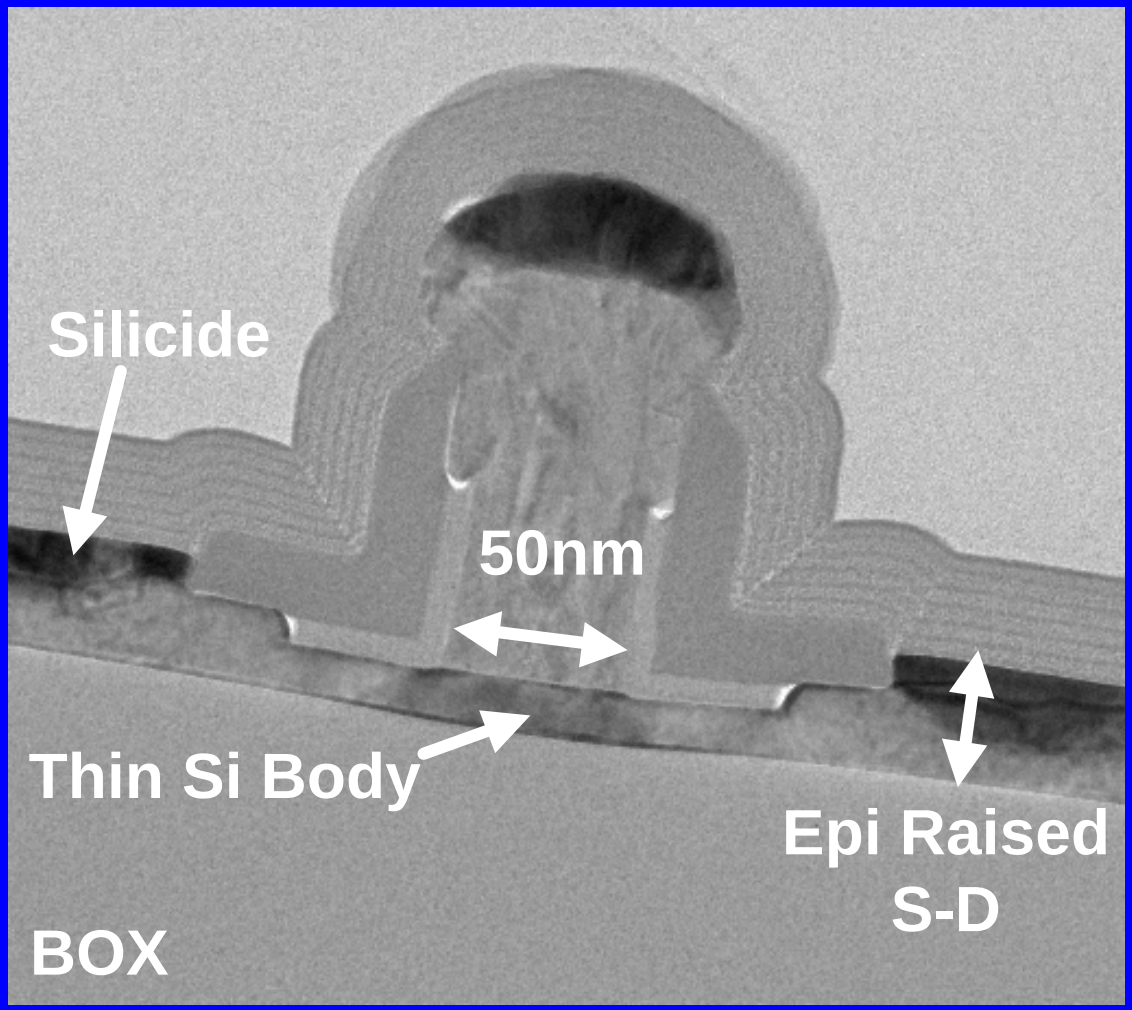
Objective of This Work

- Demonstrate sub-70nm DST has significantly better short channel effects and lower I_{OFF} than the best bulk Si and PD-SOI
- Demonstrate sub-70nm DST has significantly better transistor performance than the best bulk Si and PD-SOI
- Illustrate the need for the epi raised S-D element in the DST architecture

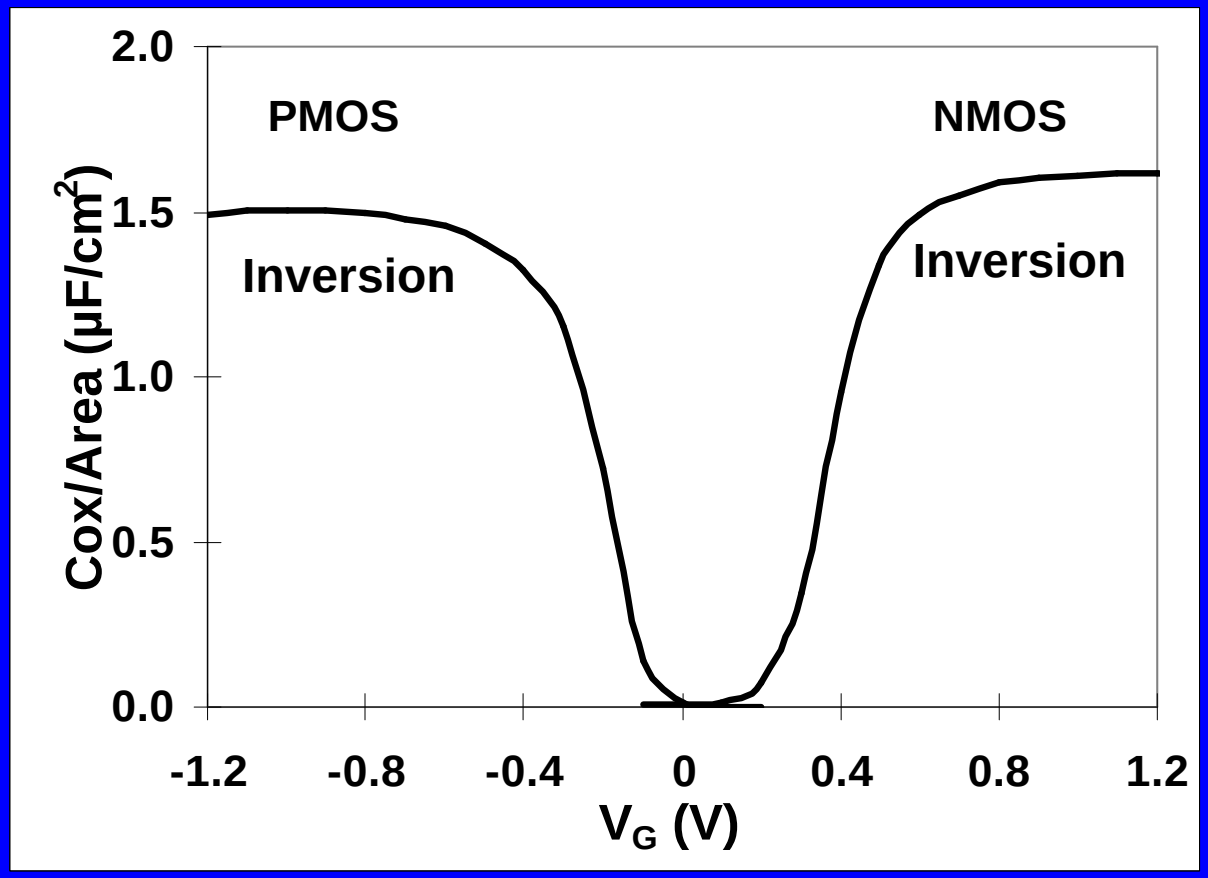
DST Process Flow for This Work

- Silicon body thickness < 30nm
- BOX thickness ~ 200nm
- Physical SiO_2 T_{OX} = 1.5nm
  - Initial work performed using SiO_2
  - High-K currently being integrated
- Sub-70nm physical gate length
- Ni or Co salicide

Depleted Substrate Transistor (DST)

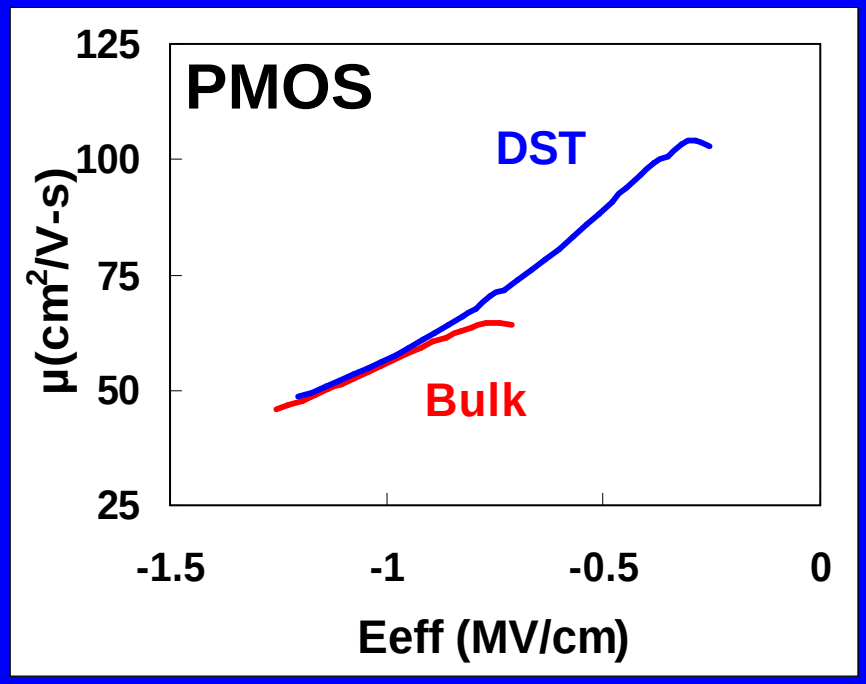


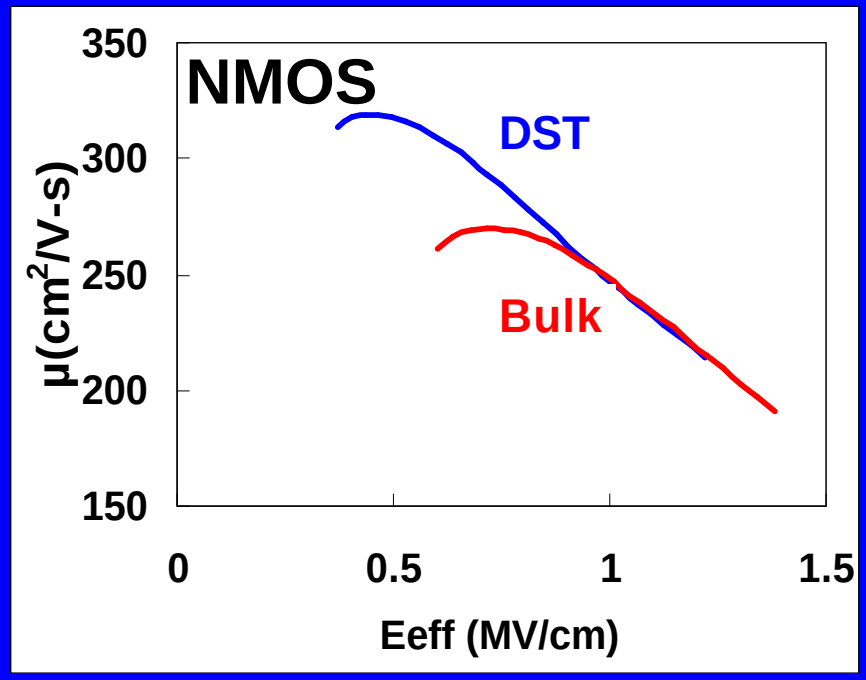
1.5nm Gate Oxide on Thin Si



No abnormality in forming ultra-thin gate oxide on thin Si body

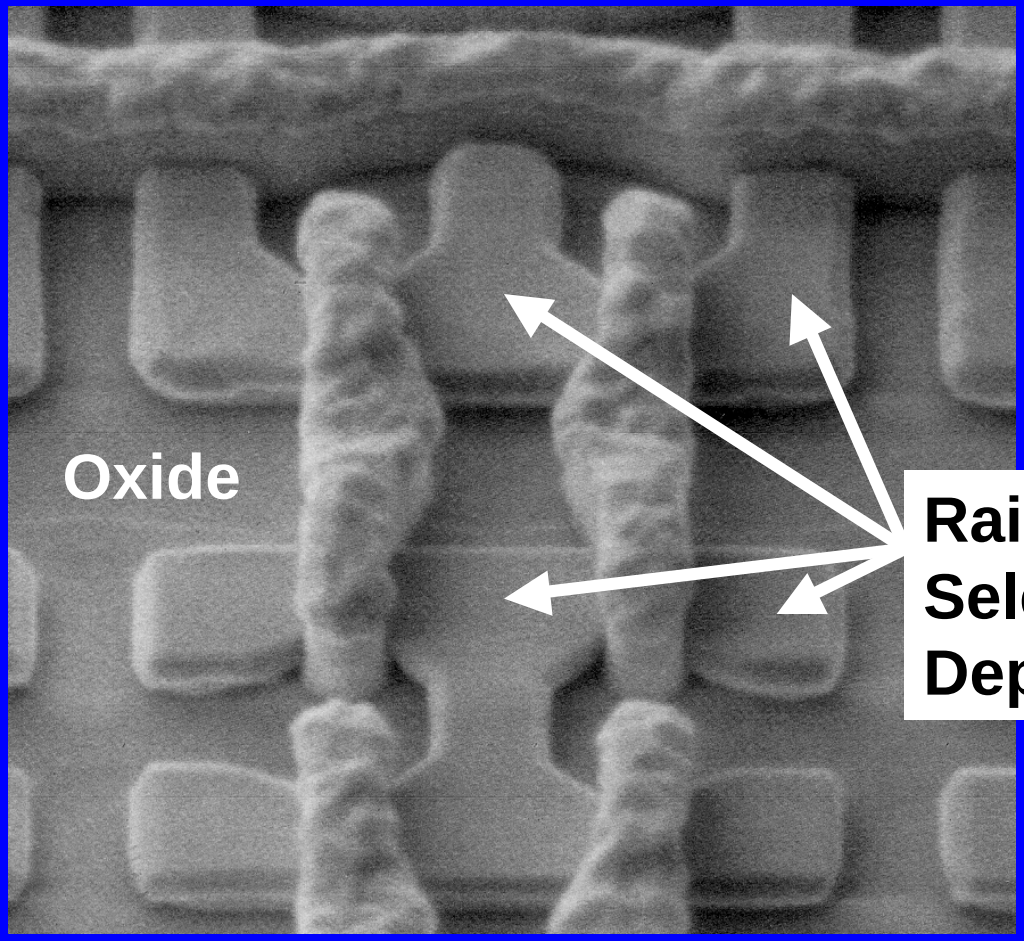
Effective Channel Mobility in Thin Si



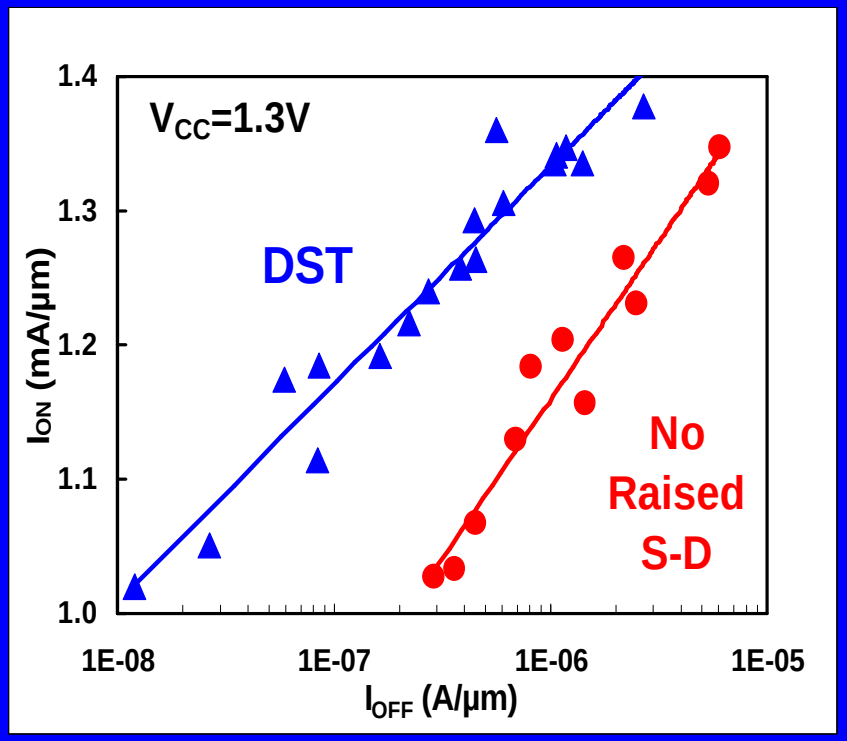


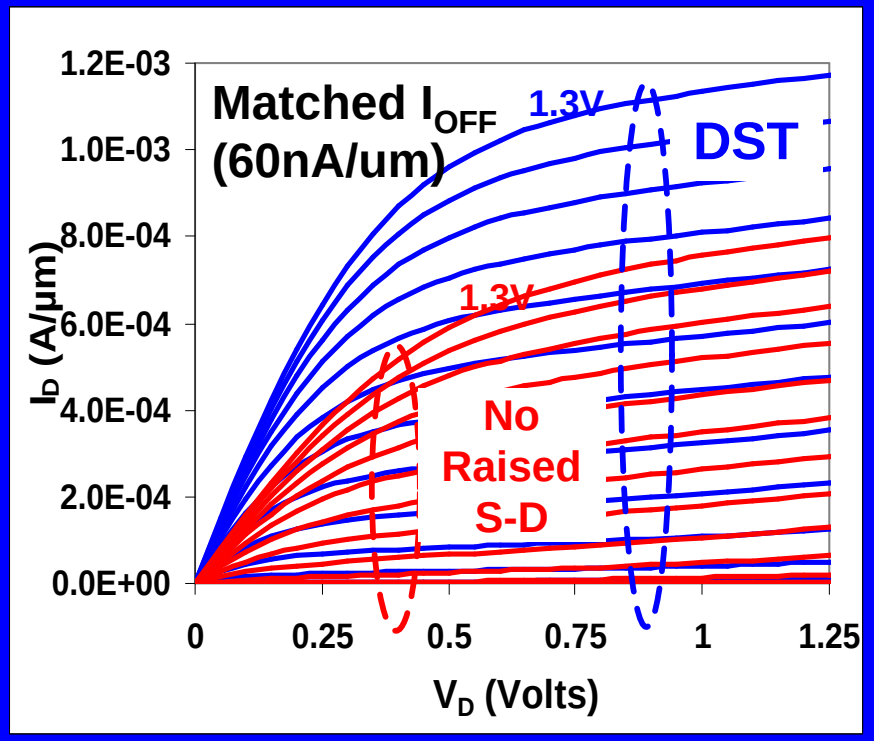
No channel mobility degradation in the thin Si body

DST Requires Raised Source-Drain



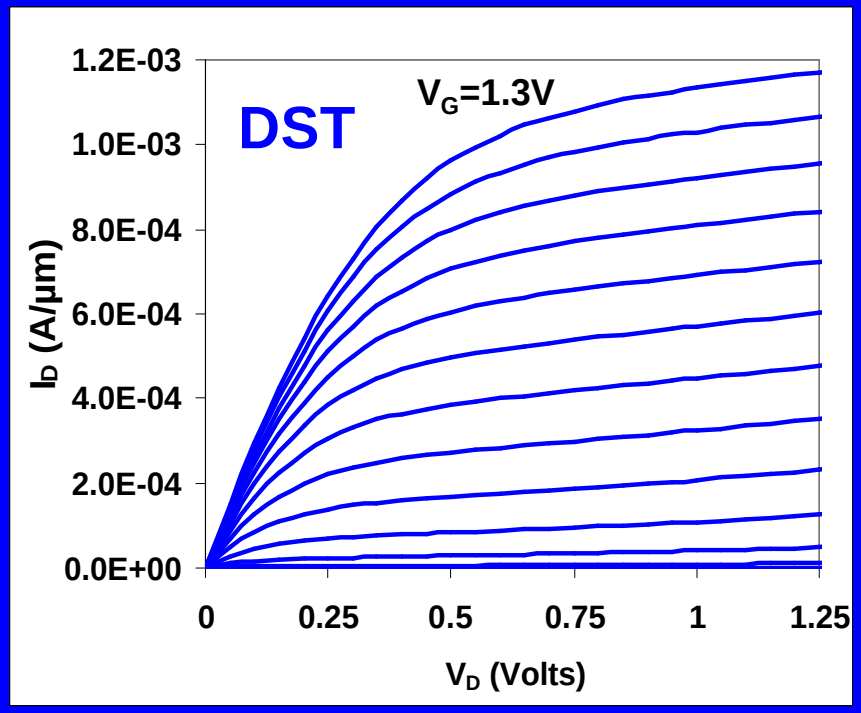
65nm N-Channel DST
(Raised S-D vs. No Raised S-D)

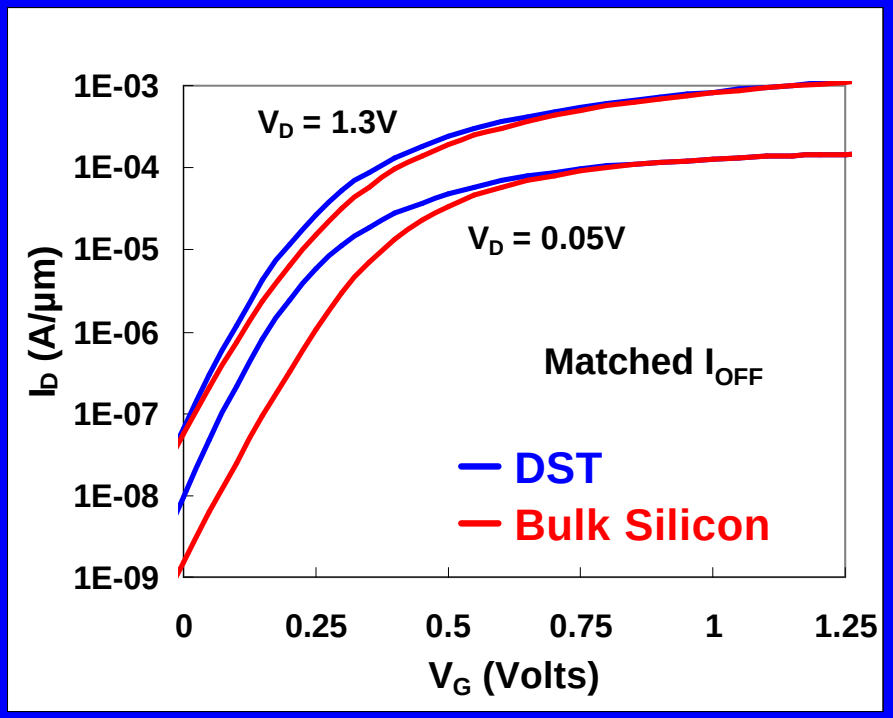




>50% I_{ON} improvement using raised S-D for same I_{OFF}= 60nA/um

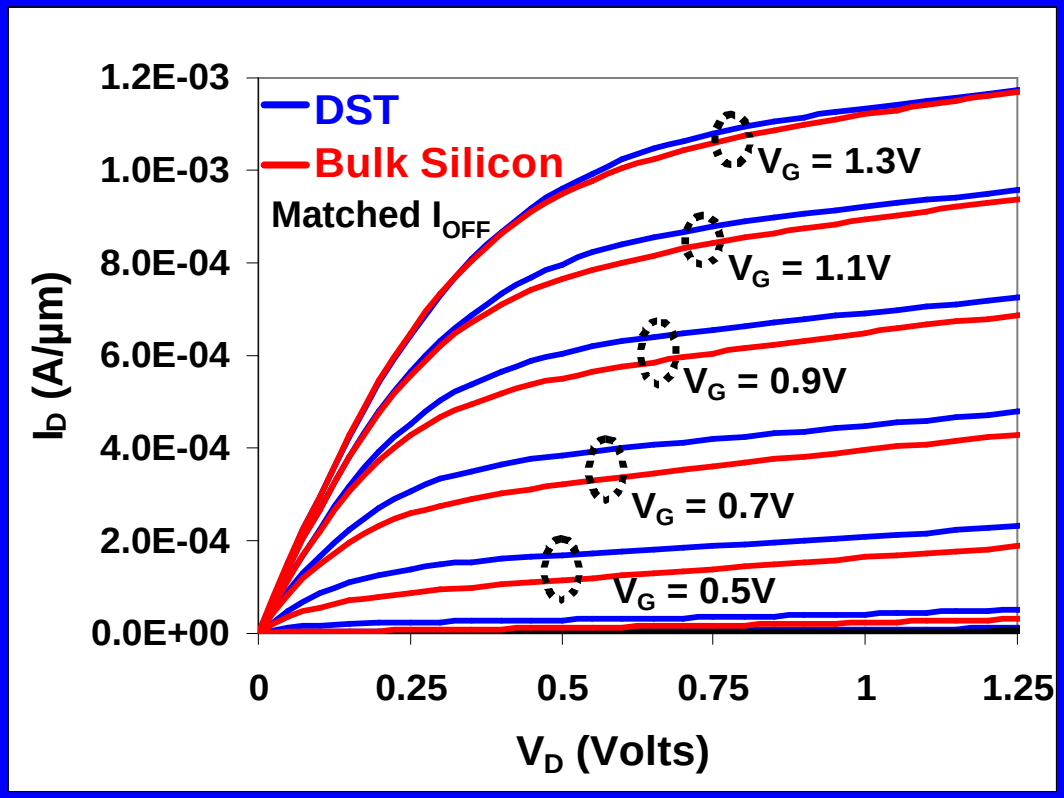
65nm N-Channel DST





- No floating body effect
- Excellent SCE: S.S. = 75mV/decade, DIBL = 45mV/V
  - for bulk Si, S.S. = 95mV/decade, DIBL = 100mV/V
- Excellent drive current
  - I_{ON} = 1.18mA/um, I_{OFF} = 60nA/um @ V_{CC} = 1.3V

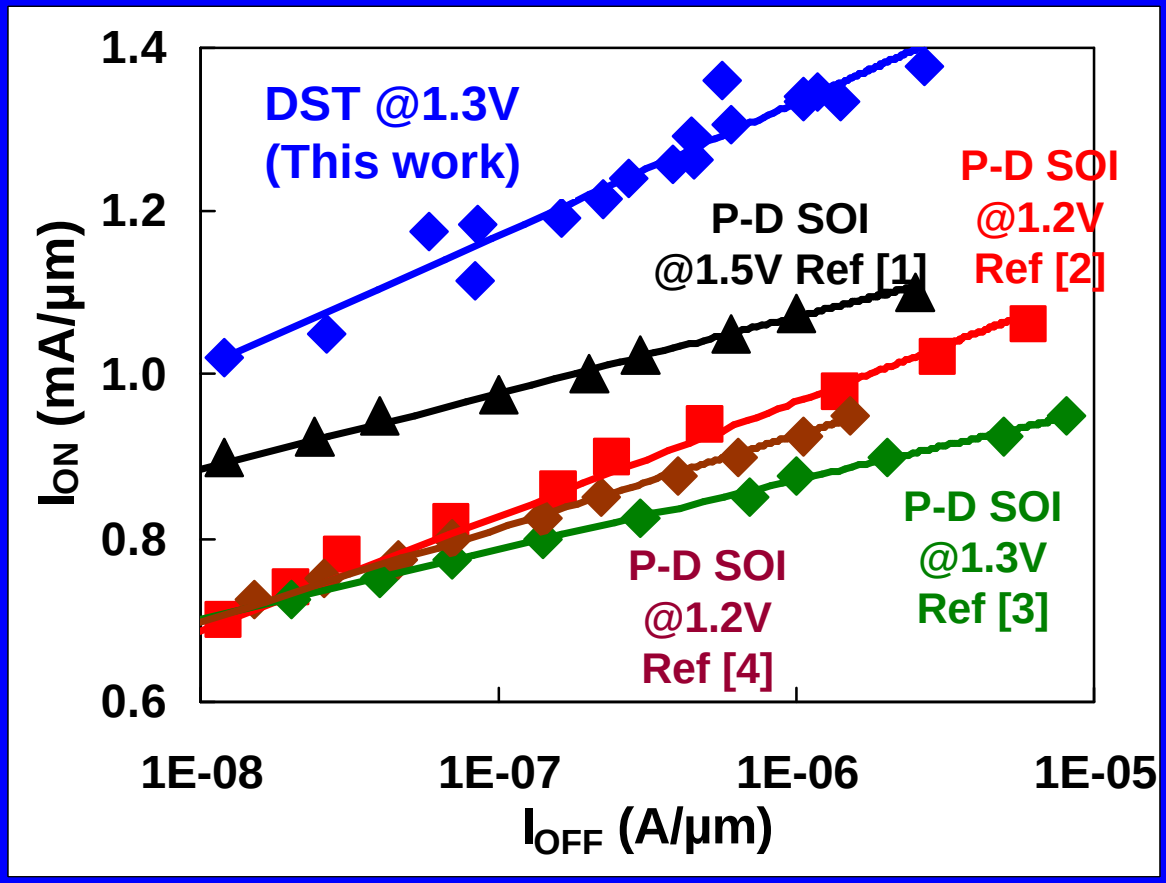
65nm N-Channel DST



DST shows improved I_D-V_D characteristics over bulk Si

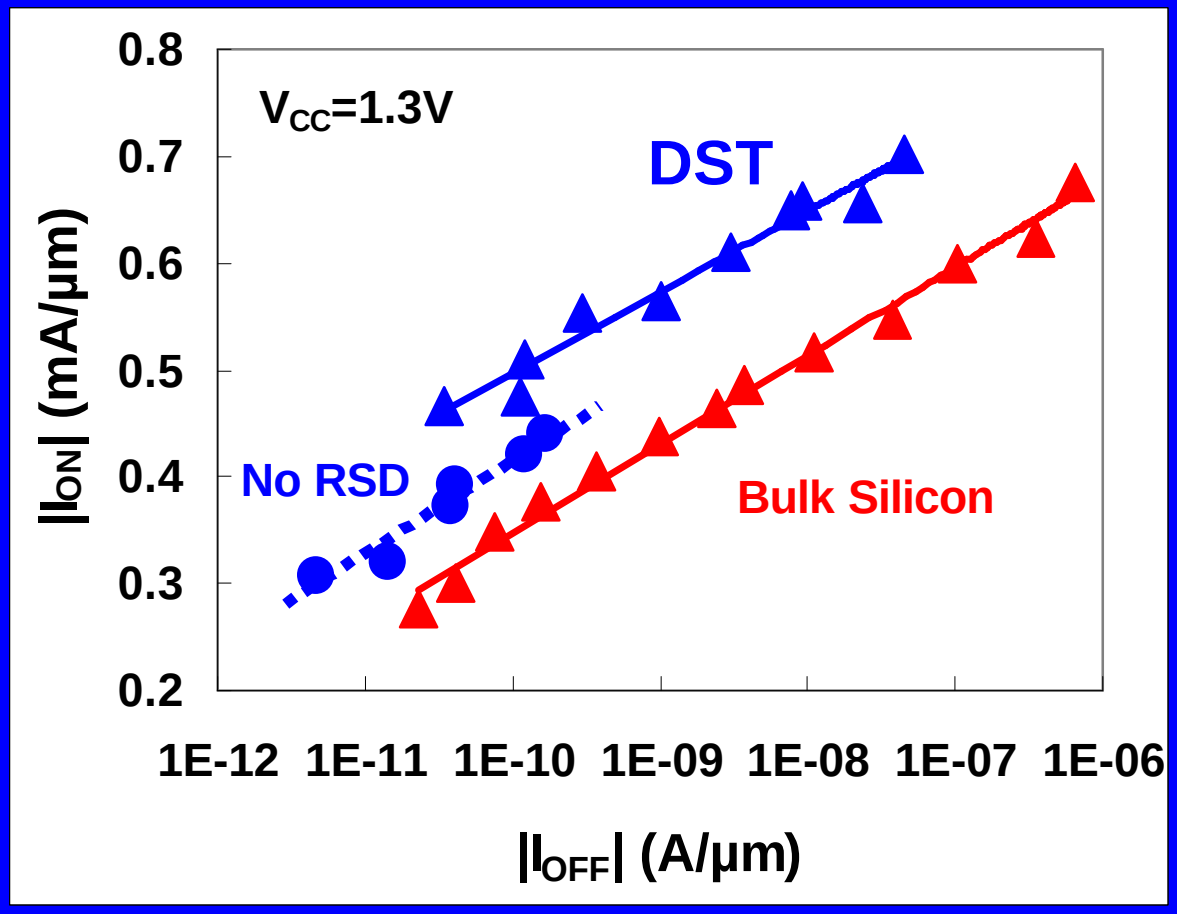
- **60% reduction in DIBL**
- **>25% improvement in S.S.**

NMOS: DST Outperforms P-D SOI by >20%



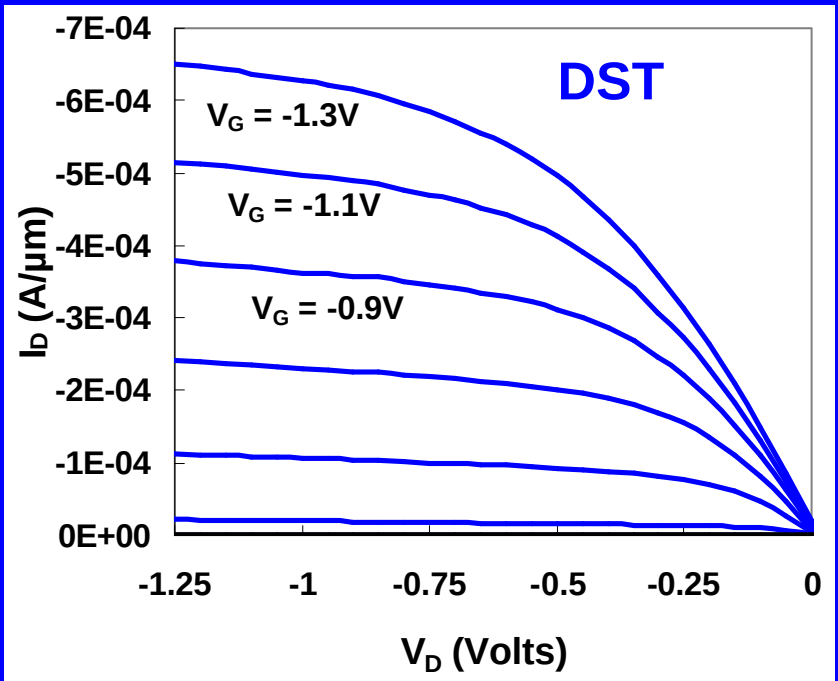
Ref [1]: I.Y. Yang et al., IEDM 1999
Ref [2]: W.P. Maszara et al., VLSI 2001
Ref [3]: K. Sukegawa et al., VLSI 2000
Ref [4]: P. Smeys et al., VLSI 2000

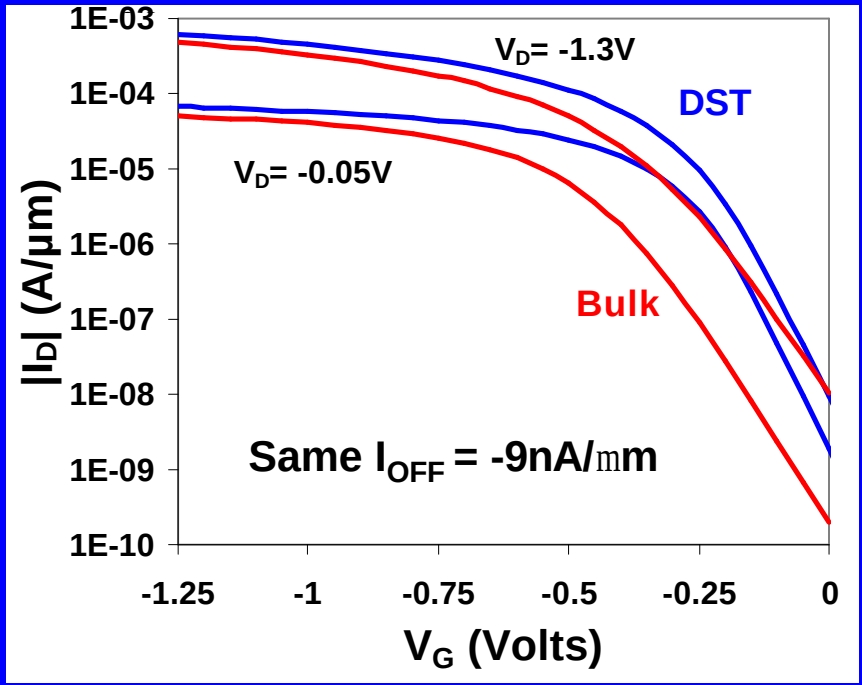
P-Channel DST



DST shows 30% higher I_{ON} than bulk Si for a given I_{OFF}

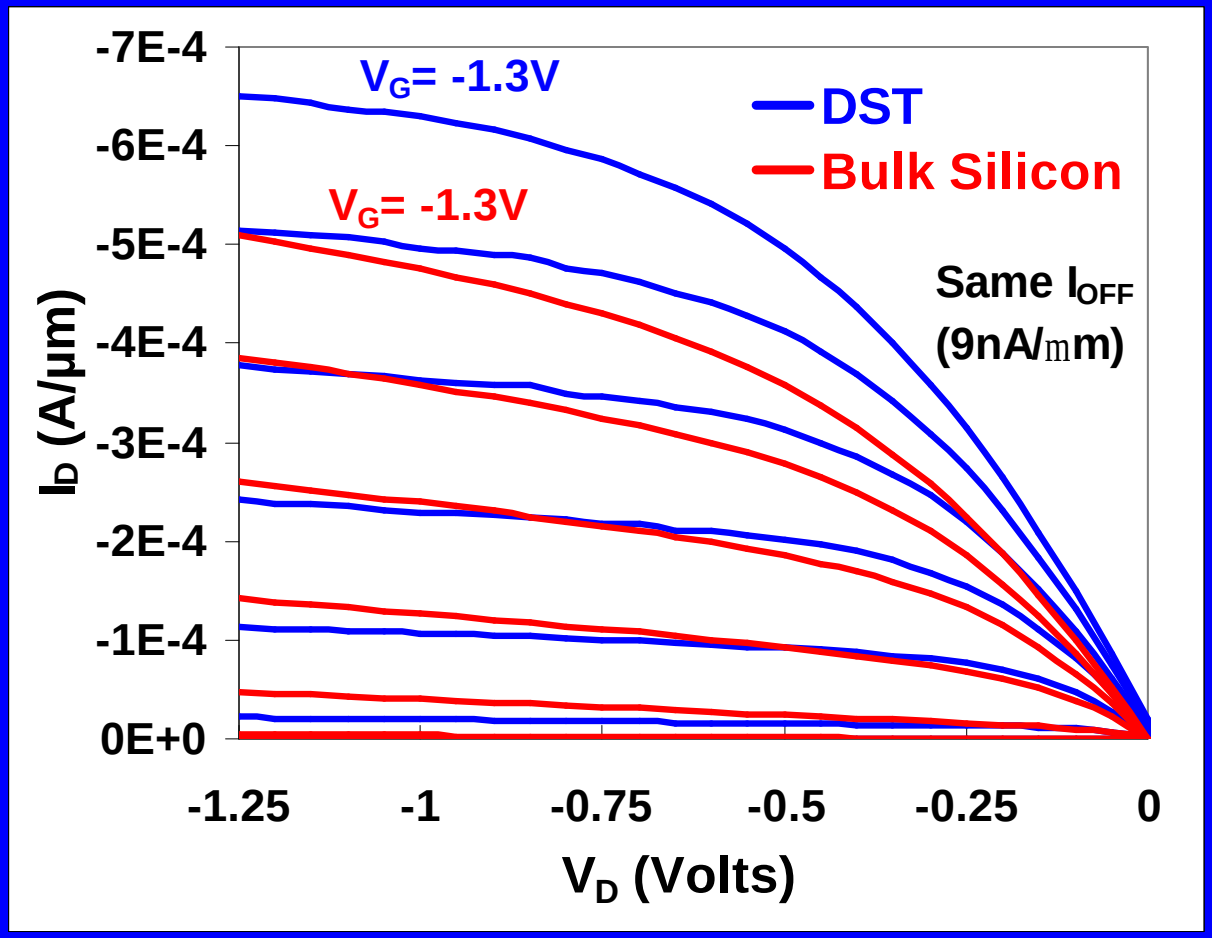
50nm P-Channel DST





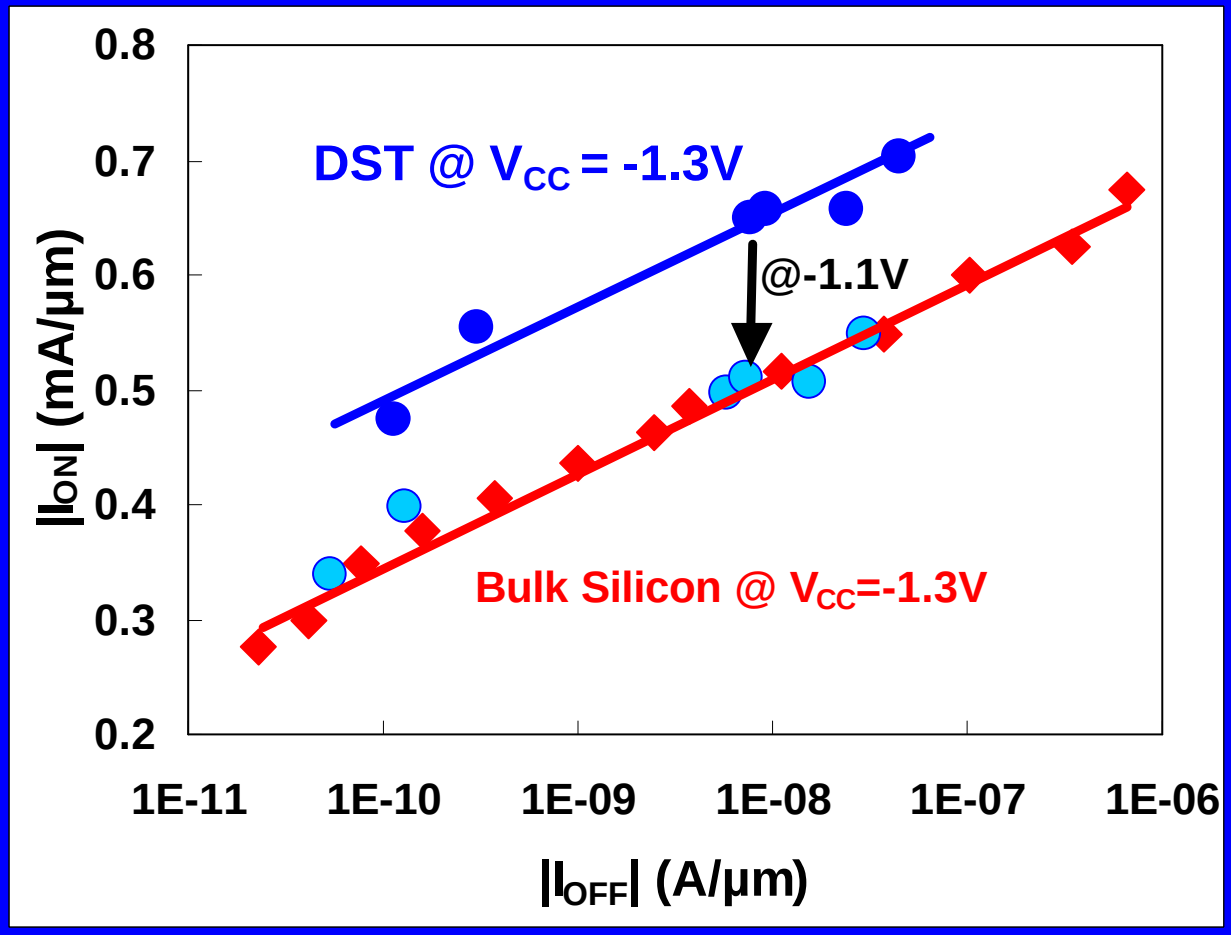
- No floating body effect
- Excellent SCE: S.S. = 70mV/decade, DIBL = 40mV/V
  - for bulk Si, S.S. = 95mV/decade, DIBL = 100mV/V
- Record-High drive current ever reported for a given I_{OFF}
  - I_{ON} = -0.65mA/um, I_{OFF} = -9nA/um @ V_{CC} = -1.3V

50nm P-Channel DST



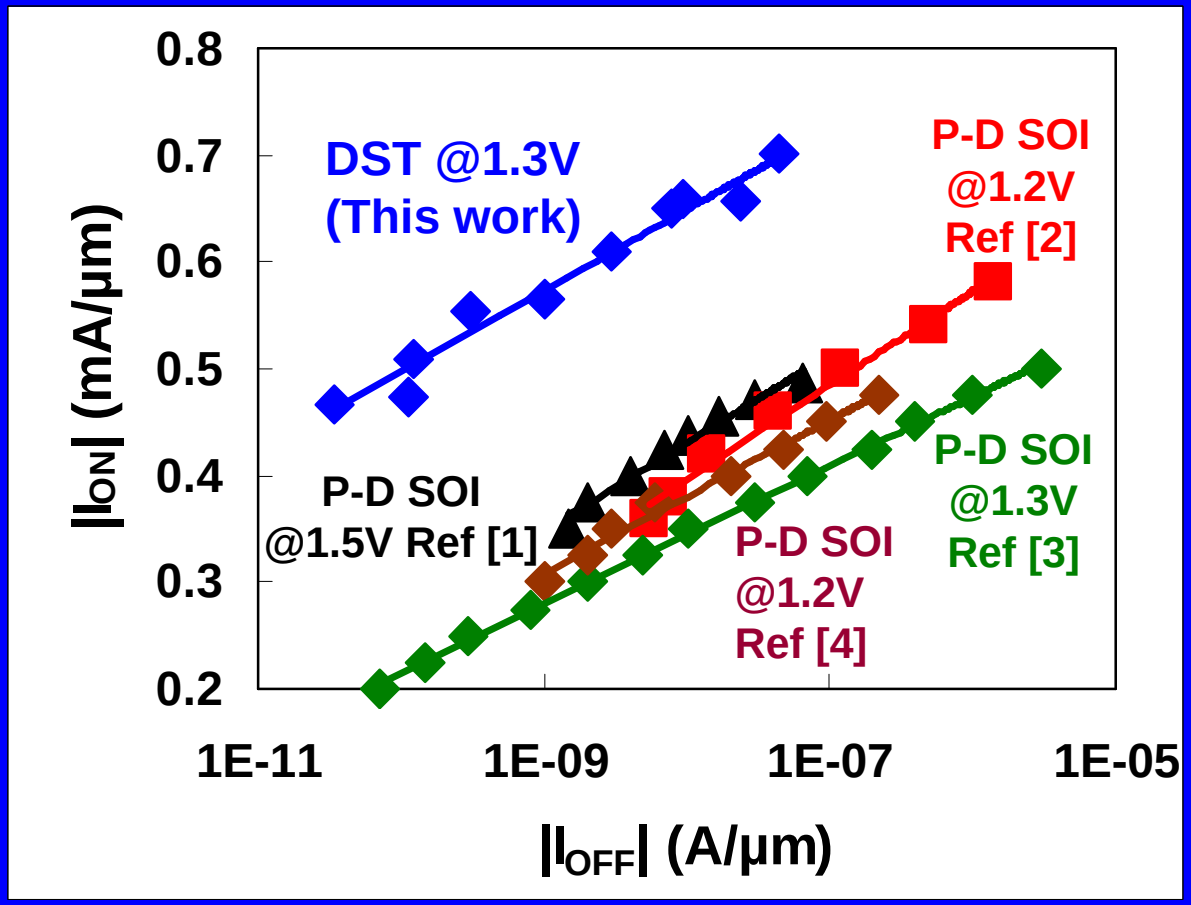
30% higher I_{ON} than bulk Si for same I_{OFF}

Power Performance



DST at -1.1V achieves identical I_{ON}-I_{OFF} performance to bulk Si at -1.3V, but with >30% power reduction

PMOS: DST Outperforms P-D SOI by >50%



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Summary

- The Depleted Substrate Transistor (DST) architecture includes
  - High-K to reduce gate leakage
  - Depleted-Si-body to improve SCE and I_{OFF}
  - Epi raised S-D to improve transistor I_{ON}
- Sub-70nm DST shows significantly better short-channel effects and lower I_{OFF} than the best bulk Si and P-D SOI
- Sub-70nm DST significantly outperforms the best bulk Si and P-D SOI in transistor drive current without the FBE

Acknowledgement

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